



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Yue-Der Chih

Examiner: Huan Hoang

Serial No.: 10/785,522

Group Art Unit: 2827

Filed: 02/24/2004

Confirmation No.: 8308

For: AN ARRAY STRUCTURE OF TWO-TRANSISTOR CELLS WITH MERGED FLOATING GATES FOR BYTE ERASE AND RE-WRITE IF DISTURBED ALGORITHM

CERTIFICATE OF MAILING/FACSIMILE TRANSMISSION PURSUANT TO 37 C.F.R. §1.8

I hereby certify that this correspondence (and anything referred to as being transmitted herewith) is being facsimile transmitted to the United States Patent and Trademark Office (Fax No. 571-273-2885) on the date shown below.

Office of Initial Patent Examination's
Filing Receipt Corrections

Date: May 12, 2006

Maria E. Provencio

Examiner Huan Hoang
Office of Initial Patent Examination's
Filing Receipt Corrections
Commissioner for Patents
5 P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR CORRECTED FILING RECEIPT

Commissioner:

10 Please make the following corrections with respect to the Filing Receipt of the above-identified application:

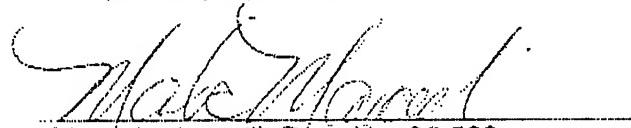
Inventor's name should be corrected from "Yeu-Der Chih" to "Yue-Der Chih".

Assignee's name should be corrected from "Taiwan Semiconductor Mnaufacturing Co." to "Taiwan Semiconductor Manufacturing Co."

Applicant points out that error in the Assignee's name was due to a typographical error on the part of the part of the USPTO and the error on the spelling of inventor Chih's name was due to a typographical error on behalf of applicant.

A copy of the Filing Receipt with annotated corrections is included herewith.

Respectfully submitted,



Mark J. Marcelli, Reg. No. 36,593
Attorney for Applicant

Dated: May 12, 2006

5

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APPL. NO.	FILING OR 371 (C) DATE	ART. UNIT	FEE REC'D	ATTY. DOCKET NO.	DRAWINGS	TOT CLMS	IND CLMS
10/785,522	02/24/2004	2818	1578	TS02-115/320	6	41	8

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CONFIRMATION NO. 8308
FILING RECEIPT



OC000000012689048

Date Mailed: 05/18/2004

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections, facsimile number 703-746-9195. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

Applicant(s) *Yue-Der*
Yue-Der Chih, Hsin-Chu City, TAIWAN;

Assignment For Published Patent Application

Taiwan Semiconductor Manufacturing Co.,

Manufacturing

Domestic Priority data as claimed by applicant

Foreign Applications

If Required, Foreign Filing License Granted: 05/17/2004

Projected Publication Date: 08/25/2005

Non-Publication Request: No

Early Publication Request: No

Title

Array structure of two-transistor cells with merged floating gates for byte erase and re-write if disturbed algorithm

Preliminary Class

365

**LICENSE FOR FOREIGN FILING UNDER
Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15**

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